

Fault Tolerant & Testable Sequential Reversible Circuit Design

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Reviews

This book is really gripping and intriguing. It is writter in easy words and never confusing. You can expect to like the way the blogger create this pdf. (Summer Jacobson)

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FAULT TOLERANT & TESTABLE SEQUENTIAL REVERSIBLE CIRCUIT DESIGN



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Condition: New. Publisher/Verlag: LAP Lambert Academic Publishing | A Designers Approach to Realize Fault Tolerant Sequential Reversible Circuit | Fast growing computing demands the power consumption and chip size issues are posing challenges for logic design with conventional technologies because of the above reliability in conventional technologies is also becoming important. Reversible computing is emerging as an alternative that offers high computation speed, high packaging density and low heat dissipation. This book expands on many of the most popular reversible computing topics such as sequential reversible building block, parity preservation and fault tolerant characteristics of sequential circuits for addressing the reliability issues. In this book, we have reported a Pareek gate suitable for low cost flip-flops design and then design methodology to develop flip-flops are incorporated. Finally, these circuits have been converted into fault tolerant circuits by preserving their parity and designs of offline as well as online testable circuits have been proposed. In addition, the text book presents the statistical results of proposed designs over quantum cost as well as other optimization parameters with existing circuits in literature and a significant improvement is achieved in almost all the parameters. | Format: Paperback | Language/Sprache: english | 76 pp.

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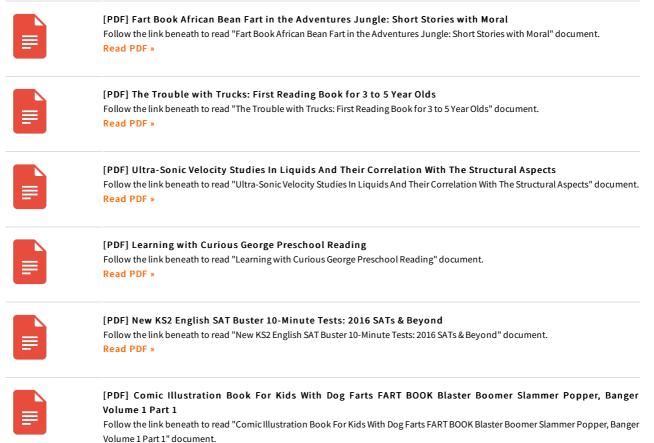
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