



Data Integrity for On-Chip Interconnects

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Condition: New. Publisher/Verlag: VDM Verlag Dr. Müller | A Communication Theoretic Approach | The desire for having a smaller-faster chip that does more than ever before, has led to shrinking feature size and growing integration density. This integration has left designers grappling with increasing concerns of signal-integrity (SI), timing- closure and power-consumption. Firstly, the shrinking feature size has resulted in greater delays. Further, the adjacent wires are now very close and cause Cross-talk to each other's signals. Traditional designs focus on protecting SI on long parallel wires. The SI designs accomodate the worst case delays of signals; while they aim to improve the worst-case delays at a circuit level using novel tricks, they are transparent to the actual data carried in the wires. Departing from this trend, this work aims to introduce an information theoretic approach to address data-integrity (DI). A novel approach for evaluating the data carrying capacity of long parallel wires is presented herein. This capacity is much greater than the data-rate achieved by SI designs. This work also proposes several practical designs with data-rate approaching this capacity. | Format: Paperback | Language/Sprache: english | 132 pp.



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