

## Cmos Circuits for Piezoelectric Energy Harvesters: Efficient Power Extraction, Interface Modeling and Loss Analysis



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### **Reviews**




*Thorough guide for pdf enthusiasts. Better then never, though i am quite late in start reading this one. Its been printed in an remarkably simple way which is only soon after i finished reading through this pdf by which really altered me, change the way i believe.*  
*(Dr. Rowena Wiegand)*

## CMOS CIRCUITS FOR PIEZOELECTRIC ENERGY HARVESTERS: EFFICIENT POWER EXTRACTION, INTERFACE MODELING AND LOSS ANALYSIS



To read **Cmos Circuits for Piezoelectric Energy Harvesters: Efficient Power Extraction, Interface Modeling and Loss Analysis** PDF, remember to access the web link listed below and save the file or have access to other information that are related to CMOS CIRCUITS FOR PIEZOELECTRIC ENERGY HARVESTERS: EFFICIENT POWER EXTRACTION, INTERFACE MODELING AND LOSS ANALYSIS ebook.

Springer, Netherlands, 2016. Paperback. Book Condition: New. 235 x 155 mm. Language: English . Brand New Book \*\*\*\*\* Print on Demand \*\*\*\*\*.This book deals with the challenge of exploiting ambient vibrational energy which can be used to power small and low-power electronic devices, e.g. wireless sensor nodes. Generally, particularly for low voltage amplitudes, low-loss rectification is required to achieve high conversion efficiency. In the special case of piezoelectric energy harvesting, pulsed charge extraction has the potential to extract more power compared to a single rectifier. For this purpose, a fully autonomous CMOS integrated interface circuit for piezoelectric generators which fulfills these requirements is presented. Due to these key properties enabling universal usage, other CMOS designers working in the field of energy harvesting will be encouraged to use some of the shown structures for their own implementations. The book is unique in the sense that it highlights the design process from scratch to the final chip. Hence, it gives the designer a comprehensive guide of how to (i) setup an appropriate harvester model to get realistic simulation results, (ii) design the integrated circuits for low power operation, (iii) setup a laboratory measurement environment in order to extensively characterize the chip in combination with the real harvester and finally, (iv) interpret the simulation/measurement results in order to improve the chip performance. Since the dimensions of all devices (transistors, resistors etc.) are given, readers and other designers can easily re-use the presented circuit concepts. Softcover reprint of the original 1st ed. 2015.

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